isolation region 3, and the second impurity region portion 50 is formed to be connected to interconnection layer 13 at the lower end of contact hole 10a. This structure enables lower resistance of the semiconductor substrate near the lower end of the semiconductor device.

This structure is not shown in the disclosed admitted prior art embodiment. Kuroda does not disclose this feature and there is nothing in the combined teachings of the prior art references that would lead the artisan to modify either device to obtain the first and second impurity region portions recited in amended claim 1.

Accordingly, it is submitted that the Amendment proposed herein renders the application in condition for allowance. Entry of the Amendment and allowance of the application are respectfully solicited. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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